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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,742	09/19/2003	Alan G. Wood	2269-6095US (03-0593.00/U	6057

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EXAMINER	
GHYKA, ALEXANDER G	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
10/10/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	10/666,742	WOOD ET AL.	
	Examiner	Art Unit	
	Alexander G. Ghyka	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/20/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-20,23-34 and 70-98* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-20 and 23-34* is/are allowed.

6)☒ Claim(s) *70-74,76-86 and 88-98* is/are rejected.

7)☒ Claim(s) *75 and 87* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

ALEXANDER GHYKA
PRIMARY EXAMINER

Au 28.2

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 8/27/07; 7/20/07
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response of 7/20/2007 has been considered and entered in the record. Claims 17-20, 23-34 and 70-98 are now under consideration. Claims 17-20 and 23-34 are allowed for the reasons as discussed below. With respect to Claims 70-74, 76-86 and 88-98, Applicants arguments have been considered but they are not persuasive for the reasons as discussed below. Claims 75 and 87 are objected to, but would be allowable if written in independent form, for the reasons as discussed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of

35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 70-74, 76-86 and 88-98 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leedy et al (US 5,869,354) in view of Grigg (US 6,562,661) and Tandy et al (US 6,524,881) for the reasons of record

Claims 70 and dependent Claims thereof generally require a method for thinning a semiconductor substrate comprising molding a support structure on an active surface of the semiconductor substrate; removing material from a back side of the semiconductor substrate to form a thinned semiconductor substrate; and transporting the thinned substrate for further processing. Claims 82 and dependent Claims thereof generally require a method for thinning a semiconductor substrate comprising forming a support structure on an active surface of the semiconductor substrate; securing the semiconductor substrate to a platen with the active surface facing the platen and the support structure abutting at least one surface or feature of or on the platen; removing material from a back side of the semiconductor substrate supported by the support structure and the platen to form a thinned semiconductor substrate; and transporting the thinned substrate for further processing.

Leedy et al disclose a method of making a dielectrically isolated integrated circuit. Leedy et al disclose the step of attaching an annular support ring to an edge portion of a semiconductor substrate on a principal side, and thinning the backside of the semiconductor substrate, as required by present claims 70-74

and 82-86. See column 7, line 50 to column 8, line 15, column 44, lines 35-50 and column 45, lines 1-5. Leedy et al also discloses the use of a package as required by present Claim 73 and 85. See the Abstract and Figures 16A –16B. As Leedy et al disclose multiple chip modules, in other words the need for further processing the thinned substrate, and therefore the limitation "transporting the thinned semiconductor substrate for further processing" is met. See Figures 32A-C for example.

However, Leedy et al does not disclose forming a layer comprising unconsolidated material over at least an outer peripheral portion of the active surface; and at least partially consolidating the unconsolidated material within at least outer peripheral regions of the layer; and forming the support structure by molding or using the platen as required by the afore mentioned Claims.

Grigg disclose stiffeners for connective structures that are configured to be secured to a semiconductor device component such as a semiconductor die or substrate by a tape automated bonding process. See the Abstract. Grigg et al disclose forming a layer comprising unconsolidated material over at least an outer peripheral portion of the active surface; and at least partially consolidating the unconsolidated material within at least outer peripheral regions of the layer, as required in present Claims 74, 83-86 and 88. See Figure 6, column 7, lines 50-60 and column 16, lines 1-15. Moreover, Grigg et al disclose energy beams as required in Claims 89-90. Furthermore, Grigg et al disclose stereolithographically forming the structure as required by present Claims 91. See column 12, line 55 to column 13, line 60.

Tandy et al disclose a method for marking a semiconductor die, which has an application in a thinning process. See Abstract. Tandy et al disclose that it is known in the art to mold support structures and it is known to use a platen 56 to provide physical support for a wafer during a backgrinding process. See Figure 1A and 2, and column 5, lines 25-40. Support structure 58, is below platen 56, and wafer 10 is on the platen, with the active side of the wafer down. The backside of the wafer, top portion is ground by 52. See Figure 2.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to bond the interconnect circuit membrane as disclosed by Leedy et al using the stiffeners as disclosed by Grigg, for their known benefit in fabricating connective structures and to arrive at the presently claimed invention. The use of a known bonding process to fabricate interconnect circuit membranes which are known in the prior art, is *prima facie* obvious. Moreover, it would have been obvious for one of ordinary skill in the art, at the time of the invention, to mold a support structure and provide a platen in a process as disclosed by Leedy et al and Grigg et al, for their known benefit in the art of forming support structures and providing physical support, respectively, as disclosed by the Tandy et al reference. As Tandy et al also pertains to supporting and/or thinning wafers, a *prima facie* case of obviousness is established. Therefore, the presently claimed limitations are obvious in view of the cited references.

Response to Applicants' Arguments

Applicants argue that with respect to the subject matter recited in independent claim 70, none of Leedy, Grigg or Tandy teaches or suggests a method that includes "molding a support structure on an active surface of the semiconductor substrate". Applicants argue that the teachings of Leedy are limited to securing a preformed structure to an active surface of a substrate, while Grigg teaches the fabrication of stiffeners on a tape substrate by use of stereolithography processes, which do not comprise molding, and Tandy teaches securing a laser markable tape to the backside 12 of a wafer.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Moreover, the Examiner notes that the cited references are not limited to the particular embodiments described in applicants' arguments. The Examiner maintains that, it would have been obvious for one of ordinary skill in the art, at the time of the invention, to mold a support structure in a process as disclosed by Leedy et al and Grigg et al, for their known benefit in the art of forming support structures, as disclosed by the Tandy et al reference. As Tandy et al also pertains to supporting and/or thinning wafers, a *prima facie* case of obviousness is established. The use of a known method, molding, for its known utility, forming a support, would have been obvious to one of ordinary skill

in the art. As all of the references pertain to making semiconductors, a *prima facie* case of obviousness is established.

With respect to the subject matter of amended independent Claim 82, Applicants argue that none of Leedy, Grigg or Tandy teaches or suggests " securing a semiconductor substrate to a platen with an active surface facing the platen and the support structure abutting at least one surface or feature of or on the platen" and "removing material from a back side of the semiconductor". The Examiner maintains that Tandy et al disclose that it is known in the art to mold support structures and it is known to use a platen 56 to provide physical support for a wafer during a backgrinding process. See Figure 1A and 2, and column 5, lines 25-40. Support structure 58, is below platen 56, and wafer 10 is on the platen, with the active side of the wafer down. The backside of the wafer, top portion is ground by 52. See Figure 2.

Applicants argue that one of ordinary skill in the art would have no reason to substitute one of the frame or ring of Leedy, the stiffeners of Grigg, and the laser markable tape of Tandy for another. The Examiner maintains that the rejection as discussed above does not entail the substitution of those components.

Allowable Subject Matter

Claims 17-20 and 23-34 are allowed.

Claims 75 and 87 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent

form including all of the limitations of the base claim and any intervening claims. The afore mentioned Claims comprise the limitation "support structure includes an outer peripheral portion that extends beyong an outer peripheral edge of the semiconductor substrate and a downwardly extending portion located laterally adjacent to the outer peripheral edge of the semiconductor substrate" *inter alia*, which is not anticipated or made obvious by the cited references.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander G. Ghyka whose telephone

number is (571) 272-1669. The examiner can normally be reached on Monday through Friday during general business hours. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGG
September 27, 2007

ALEXANDER GHYKA
PRIMARY EXAMINER

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